UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/576,056 | 05/23/2000 | David Gordon Ballinger | 30019.100USU1 | 3531 |

23552 7590 11/19/2003

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

| EXAMINER | |
|---|---|
| PATHAK, SUDHANSHU C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2634 | 5 |

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/576,056 | BALLINGER, DAVID GORDON | |
| | Examiner | Art Unit | |
| | Sudhanshu C. Pathak | 2634 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23rd May, 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *55 and 56* is/are allowed.

6)☒ Claim(s) *1-44,46-48,50 and 52-54* is/are rejected.

7)☒ Claim(s) *45, 49, 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23rd May, 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

1. Claims 1-to-56 are pending in the application.

### *Drawings*

2. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. This comment is regarding Fig. 9.

3. Figures 3, 4 & 7, which illustrate the various embodiments of the invention, are extremely hard to read and locate the elements as described in the specification. Furthermore, there are no arrows used to indicate the direction of data (signal) flow between the interconnecting elements of the system.

   Appropriate correction is required.

4. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 & 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (5,093,841) in view of Cui et al. (6,111,910).

Regarding to Claims 1 & 10, Vancraeynest discloses a circuit and method for synchronizing the local receiver clock to an arriving chip stream in a spread spectrum communication system (Column 2, lines 45-60 & Column 5, lines 20-24). Vancraeynest further discloses correlating the incoming digital chip stream with a reference sequence, at each chip time period (Column 5, lines 33-46). The indication that a particular local clock phase is valid is determined by correlating over multiple bit periods, more specifically Vancraeynest uses "2M" bit periods where "M>1" (Column 6, lines 7-44 & Column 3, lines 16-36 & Column 2, lines 62-68) where "M" is defined as all the possible phases of the local synchronizing clock (Column 4, lines 4-7 & Column 3, lines 20-23 & Claim 7). However Vancraeynest does not specify maintaining and using the history of previous correlations in synchronizing the bit clock.

Cui discloses an apparatus for demodulating a received signal in a cellular communication system. Cui discloses in his invention using a demodulator that can use history correlation data to extract the modulating symbols from the received signals (Abstract, lines 1-14 & Column 3, lines 29-31). Cui also discloses a method of estimating the information signal by correlating the received signal with all the possible reference signals, and selecting as an estimate the reference signal whose correlation with the received signal most closely resembles a weighted average of the correlations between previously estimated information signals and their corresponding received signals (Column 3, lines 39-57 & Column 6, lines 43-58 & Column 12, Claim 7 & Fig. 4). Cui further discloses using a clock to sample the

reference signal, which can be modified such that the phases at which the samples of the reference signal are generated match the phase at which the received signal is sampled (Column 12, lines 7-15 & Fig. 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by maintaining a history of the correlations and further using the history of the correlations as described by Cui to synchronize the local clock in the apparatus and method as described by Vancraeynest a more accurate estimate of the reference sequence is obtained and further makes the receiver immune to instantaneous noise spikes further providing a more accurate synchronization between the transmitter and the receiver.

7. Claims 2-4, 6, 8, 11, 13, 15, 19, 23, 25, 27, 29, 33, 35, 37-38, 40-44, 46-47 & 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (5,093,841) in view of Cui et al. (6,111,910) in further view of Bustamante et al. (5,375,140).

Regarding to Claims 2-4, 6, 8, 11, 13, 15, 19, 23, 25, 27, 29, 33, 35, 37-38 & 40, Vancraeynest in view of Cui discloses a method and apparatus for synchronizing the local receiver clock to an arriving chip stream in a spread spectrum communication system; correlating the incoming digital chip stream with a reference sequence, at each chip time period and further synchronizing a bit clock by using the history of the correlations as described above. Vancraeynest also discloses a threshold for comparing the correlator output to the threshold and generating a threshold correlator output (Column 1, lines 42-57). Vancraeynest further discloses that an

indication of valid or invalid for each phase is obtained based on the relative timing of correlation threshold crossings obtained for each phase (Column 3, lines 57-61 & Fig. 1b), furthermore when the number of matches exceeds a predetermined upper correlation threshold a data detection decision is made indicating a synchronization (Column 1, lines 45-48 & Column 3, lines 64-68 & Column 4, lines 1-25 & Fig. 1b). However, these references do not specify histogramming the correlator output over all possible sample positions or over a finite window of the sample positions for the bit clock.

Bustamante discloses a wireless (spread spectrum) telephone system for a combination of a base station unit a multiple handsets (Column 2, lines 13-16) in a short-range mobile environment where significant multipath fading exists (Abstract, lines 1-4). Bustamante discloses using a histogram to observe correlator output of the power profile to determine the peak power measure and verify that it meets a certain threshold (Column 15, lines 20-63). Bustamante further discloses that the histogram is done over a finite window of symbols and is reset every frame (Column 15, lines 55-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that histogramming the correlator output as described by Bustamante to the correlator output as described in the system described by Vancraeynest in view of Cui would provide the ability to observe the correlator results and make a decision in regards to the phase of the receiver local clock based on the comparison of the weighted correlator average with the threshold value. There is no criticality in histogramming over all possible samples or over a finite

window of samples, since all possible samples can be considered a defined window of finite samples, and this is a matter of design choice depending on the computing power or storage capacity in the receiver. Furthermore, histogramming the correlator over a bit period or multiple bit period is a design choice, since Vancraeynest computes the correlation over more than two bit periods depending on all the possible phases of the local synchronizing clock.

Regarding to Claims 41, 42, 43, 44, 46, 47, 53 & 54, Vancraeynest in view of Cui discloses a method and apparatus for synchronizing the local receiver clock to an arriving chip stream in a spread spectrum communication system; correlating the incoming digital chip stream with a reference sequence, at each chip time period and further synchronizing a bit clock by using the history of the correlations as described above. Vancraeynest further discloses the clock recovery circuit comprising a correlator (Fig. 3, element 103) for correlating a reference PN-sequence with the received chip stream (Column 6, lines 45-63), a phase controller (Fig. 3, elements 112, 114, 116, 130 & 160) coupled to the correlator, being configured and arranged to the correlator output, and a bit clock generator (Fig. 3, element 110) coupled to the phase controller, for generating a bit clock and output of the correlator to select/adjust the phase of the bit clock generator (Column 7, lines 1-68 & Column 8, lines 1-68). Vancraeynest further discloses a plurality of counters (Fig. 3, elements 140 & 150) at the correlator output used to determine weather the current phase of the bit clock is valid or invalid (Column 7, lines 45-47), furthermore the counters are asserted and incremented when a threshold correlator generates a spike (Column 7,

lines 24-68 & Column 8, lines 1-68). Vancraeynest further discloses that an indication of valid or invalid for each phase is obtained based on the relative timing of correlation threshold crossings obtained for each phase (Column 3, lines 57-61 & Fig. 1b), furthermore when the number of matches exceeds a predetermined upper correlation threshold a data detection decision is made indicating a synchronization (Column 1, lines 45-48 & Column 3, lines 64-68 & Column 4, lines 1-25 & Fig. 1b). Cui also discloses a method of estimating the information signal by correlating the received signal with all the possible reference signals, and selecting as an estimate the reference signal whose correlation with the received signal most closely resembles a weighted average of the correlations between previously estimated information signals and their corresponding received signals (Column 3, lines 39-57 & Column 6, lines 43-58 & Column 12, Claim 7 & Fig. 4). However, these references do not specify histogramming the correlator output to adjust the phase of the bit clock, over all possible sample positions or over a finite window of the sample positions for the bit clock.

Bustamante discloses a wireless (spread spectrum) telephone system for a combination of a base station unit a multiple handsets (Column 2, lines 13-16) in a short-range mobile environment where significant multipath fading exists (Abstract, lines 1-4). Bustamante discloses using a histogram to observe correlator output of the power profile to determine the peak power measure and verify that it meets a certain threshold (Column 15, lines 20-63). Bustamante further discloses that the histogram is done over a finite window of symbols and is reset every frame (Column

15, lines 55-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that histogramming the correlator output as described by Bustamante to the correlator output as described in the system described by Vancraeynest in view of Cui would provide the ability to observe the correlator results and make a decision in regards to the phase of the receiver local clock based on the comparison of the weighted correlator average with the threshold value. Furthermore, histogramming and using previous correlator values provides the system to ignore the instantaneous noise spikes thus preventing the incorrect estimation of the phase of the incoming received samples. There is no criticality in histogramming over all possible samples or over a finite window of samples, since all possible samples can be considered a defined window of finite samples, and this is a matter of design choice depending on the computing power or storage capacity in the receiver.

8. Claims 5, 7, 9, 12, 14, 16-18, 20-22, 24, 26, 28 & 30-32, 34, 36, 39, 48, 50 & 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (5,093,841) in view of Cui et al. (6,111,910) in further view of Bustamante et al. (5,375,140) in further view of Sawahashi et al. (5,768,306).

Regarding to Claims 5, 7, 9, 12, 14, 16-18, 20-22, 24, 26, 28 & 30-32 & 34, Vancraeynest in view of Cui in further view of Bustamante discloses a method and apparatus for synchronizing the local receiver clock to an arriving chip stream in a spread spectrum communication system; correlating the incoming digital chip stream with a reference sequence, at each chip time period and further synchronizing a bit

clock by using the history of the correlations, histogrammed continuously, as described above. Vancraeynest also discloses a threshold for comparing the correlator output to the threshold and generating a threshold correlator output (Column 1, lines 42-57). Vancraeynest further discloses that an indication of valid or invalid for each phase is obtained based on the relative timing of correlation threshold crossings obtained for each phase (Column 3, lines 57-61 & Fig. 1b), furthermore when the number of matches exceeds a predetermined upper correlation threshold a data detection decision is made indicating a synchronization (Column 1, lines 45-48 & Column 3, lines 64-68 & Column 4, lines 1-25 & Fig. 1b). However, these references do not disclose low pass filtering or using an accumulator to the correlator output.

Sawahashi discloses a correlator apparatus for establishing initial synchronization between the received signal and the receiver (Abstract, lines 1-20). Sawahashi also discloses the output of the correlator is directly input into a plurality of accumulators (Fig. 4, element 46 & Fig. 6, element(s) 57). Sawahashi further discloses low pass filtering the correlator output (Fig. 2, element(s) 26 & 27). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the low pass filter and the accumulator as described in Sawahashi can be implemented in the system described by Vancraeynest in view of Cui in further view of Bustamante so as to satisfy the limitations of the claims.

Regarding to Claims 48, 50 & 52, Vancraeynest in view of Cui in further view of Bustamante discloses a method and apparatus for synchronizing the local receiver

clock to an arriving chip stream in a spread spectrum communication system; correlating the incoming digital chip stream with a reference sequence, at each chip time period and further synchronizing a bit clock by using the history of the correlations, histogrammed continuously, as described above. Vancraeynest further discloses that an indication of valid or invalid for each phase is obtained based on the relative timing of correlation threshold crossings obtained for each phase (Column 3, lines 57-61 & Fig. 1b), furthermore when the number of matches exceeds a predetermined upper correlation threshold a data detection decision is made indicating a synchronization (Column 1, lines 45-48 & Column 3, lines 64-68 & Column 4, lines 1-25 & Fig. 1b). However, these references do not disclose low pass filtering or using an accumulator to the correlator output.

Sawahashi discloses a correlator apparatus for establishing initial synchronization between the received signal and the receiver (Abstract, lines 1-20). Sawahashi also discloses the output of the correlator is directly input into a plurality of accumulators (Fig. 4, element 46 & Fig. 6, element(s) 57). Sawahashi further discloses low pass filtering the correlator output (Fig. 2, element(s) 26 & 27). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the low pass filter and the accumulator as described in Sawahashi can be implemented in the system described by Vancraeynest in view of Cui in further view of Bustamante so as to satisfy the limitations of the claims.

***Allowable Subject Matter***

9. Claims 45, 49 & 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 55 & 56 are allowed over the prior art of record because the cited references do not contain the specified limitation of a receiver comprising a computer program storage medium for executing a computer process for transmitting and receiving the encoded data.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703) 305-0341. The examiner can normally be reached (Monday-Friday from 8:30 AM to 5:30 PM).

    If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

    Any response to this action should be mailed to: Commissioner of Patents and Trademarks Washington, D.C. 20231

    Or faxed to: -

    (703) 872-9314 (for Technology Center 2600 only)

    Hand-delivered responses should be brought to Crystal Part II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600